Abstract

Low power VLSI is a promising area for developing advanced wireless communication systems. The optimum word length selection for each signal in algorithm is crucial for low power design. This paper proposes a scheme for Word Length Optimization (WLO) using system level parameters such as dynamic range and SNR. The Blind Adaptive Equalizer for channel equalization is optimized with the proposed technique for fixed point implementation in VHDL. Simulation is carried out in MATLAB and also VHDL. Considering IEEE 802.16 wireless broadband network and DSL cable modem standards, the results are validated for Energy per Symbol to Noise density (Es/No) values 8 dB and 12 dB. Power saving up to 34% is observed for Xilinx’s Virtex-6 FPGAs, in comparison with conventional implementation. The result shows promising direction of optimization with good scope of automation for low power wireless applications. The suitability of adopted WLO scheme in the context of High Level Synthesis (HLS) is discussed.

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Index Terms

Computer Science Algorithms

Keywords

WLO VLSI Equalization HLS FPGA SNR Accuracy Dynamic Range;