Abstract

In this paper, we realize a high performance arithmetic circuits which is faster and have lower power consumption using a new dynamic logic family of CMOS and to analyze its performance for arithmetic circuits. This new dynamic logic family is known as Dynamic Current Mode Logic (DyCML). DyCML circuits combine the advantages of MOS current mode logic (MCML) circuits with those of dynamic logic families to achieve high performance at a low-supply voltage with low-power dissipation. A major advantage of the DyCML is the dynamic current source, which achieves smaller delays compared to the basic MCML circuits. Other advantages inherited from MCML are high performance and robustness to supply voltage scaling. DyCML gates reduce power dissipation by reducing the output voltage swing. We compare a set of arithmetic circuits implemented in Dynamic Current Mode Logic with the other dynamic logic styles. Simulation and test results show that DyCML circuits are superior to DDCVS logic styles in terms of power dissipation. A 2-bit multiplier, full adder & xor/xnor gate in DyCML style is fabricated in 180nm CMOS technology. 2-bit multiplier and a full adder dissipate 145. 1 µW and 55. 14 µW respectively at 40 MHz for a voltage swing of 1. 2V in DyCML style.
Dynamic Current Mode Logic Realization of Digital Arithmetic Circuits


Index Terms

Computer Science
Circuits And Systems

Keywords
CMOS integrated circuits  current mode logic  digital circuits  low-power integrated circuits and logic design.