Abstract

The work aims the designing and implementing an efficient HDLC chip. We use pipelining technique in HDLC register module which increases the throughput of the system and also helps in decreasing the delay of the system. In pipeline technique, number of instructions has been executed at the same time. The HDLC chip designed here supports two way communications means it supports full duplex communications which means that it can transmit and receive continuously. In this paper we adopt Xilinx’s Spartan-3E for HDLC implementation and for hardware simulation we use Modelsim SE 6. 2C.

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Index Terms

Computer Science

Wireless
Keywords
Cloud Computing  Billing  SaaS  PaaS  IaaS