Abstract

In this paper, a technique was proposed to protect memory cells, which are more susceptible to soft errors. These memory cells are to be protected with effective error correction codes. MLD codes are suitable for memory applications because of their ability to correct large number of errors. Conversely, they increase the average latency of the decoding process because it depends upon the code size that impacts memory performance. A method was proposed as majority logic decoder/detector of Euclidean geometry low density parity check codes (EG-LDPC). BUT this MLDD reduces the decoding time, memory access time and area utilization. In this brief, we obtain the application of MLDD to a class of EG-LDPC. The simulation results show that MLDD consumes less area and speed of execution is high for error detection and correction. On comparison with MLD, MLDD provides high speed of operation with reduced execution time, decreased area and high performance.
- Error Detection in Majority Logic Decoding of Euclidean Geometry Low Density Parity Check (EG-LDPC) Codes by Pedro Reviriego, Juan A. Maestro, and Mark F. Flanagan. IEEE transactions on very large scale integration (VLSI) systems, vol. 21, no. 1, January 2013.
- Performance study of Non-binary LDPC Codes over GF (q) V. S. Ganepola1, R. A. C. Carrasco1, I. J. Wassell2 and S. Le Goff1 School of Electrical, Electronic and Computer Engineering, University of Newcastle Computer Laboratory, University of Cambridge.

**Index Terms**

Computer Science circuits and systems

**Keywords**

Error correcting codes   Euclidean geometry low density parity check codes (EG-LDPC)

majority logic decoder/detector (MLDD).