Abstract

Energy efficiency is a supreme design concern in many ultralow-power applications. In such applications, high density Static Random-Access Memory (SRAM) plays a significant role. This paper explores and analyzes 1Mb SRAM array structures for energy efficiency improvement by adopting circuit modifications and inclusion of charge sharing circuits. The analysis shows that the array structure optimization and charge accumulator circuits can improve the energy efficiency for the same SRAM bit density and the same supply voltage.

References

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Index Terms

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Six-transistor (6T) Static Random-Access Memory (SRAM)  energy efficiency  minimum energy  SRAM  charge-share