Abstract

In recent days advanced digital process demands more sophisticated parameters such as throughput, power and area. It is very difficult to maintain high throughput while maintaining optimum power consumption and cell area. In most of the digital systems multipliers are deciding their performance in terms of above parameters. In the present work high speed Vedic multipliers are designed with pipeline technology. As the MAC speed is decided by Vedic Multiplier, in the present paper Multiplier and Accumulator (MAC) is designed with two way pipeline technology to meet high throughput. Vedic Multipliers are used in designing MAC unit as they are fast multipliers and further enhancing the data speed. The MAC is implemented with Cadence Encounter(R) RTL Compiler.

References


Index Terms

Computer Science Circuits And Systems

Keywords

Vedic Multiplier Throughput MAC data rate Cadence Pipeline Parallel processing