Abstract

Reversible logic is one of the promising research areas in low power applications such as quantum computing, optical information processing and low power CMOS design. In this paper we present a reversible carry look ahead adder and an array multiplier. The circuits are designed such that they result in less garbage outputs, constant inputs, and less gate count compared to previous existing designs. We also gain better improvements in terms of power and area when compared to conventional adders and multipliers. The implemented designs are simulated using NC launch and synthesized by RTL compiler.
References

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Index Terms

Computer Science
Circuits And Systems
**Keywords**

Reversible  Garbage constant  Garbage output.