Abstract

The aggressive technology scaling in VLSI leads to decrease the size of chip. Such continual miniaturization of VLSI devices has strong impact on interconnects in several ways. Interconnects in high speed applications suffer from crosstalk, signal delay and ground noise, causing degradation of system performance. Thus interconnects are becoming a limiting factor in determining circuit performance. This paper presents a comparative study on different interconnect circuit techniques for on chip interconnects. We have compared different circuit structure by placing on RC and RLC interconnects. In this delay benefit for current sensing increases with an increase in wire width. Unlike repeaters, current sensing does not require placement of buffers along the wire and it eliminates any placement constraints. Out of all these techniques a differential RLC current mode signaling circuit insertion has offered the less amount of energy. All the circuits are simulated and compared different parameters such as power, delay and energy by using micro wind in 45nm technology.

References

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A Comparative Study of Interconnect Circuit Techniques for Energy Efficient On-Chip Interconnects

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Index Terms

- Computer Science
- Circuits And Systems

Keywords

- Interconnect
- repeaters
- wire
- Current mode
- differential signaling
- clamped bit line Sense Amplifier
- energy dissipation.