New military communications require increased versatility for the transmission of a wide range of data, voice and images. There are many algorithms needed for communication like FFT (Fast Fourier Transform), DCT (Discrete Cosine Transforms), Viterbi coders and decoders, trellis techniques etc. Advances in VLSI technology continue to improve the quality of algorithm that can be implemented on a single die. But even though all these algorithms implementable on a single chip, they require large amount of computation and consequently require large die area and high levels of power dissipation. In wireless communication, Viterbi decoder which consumes more power plays an important role in communication applications. Viterbi decoder is used to decode the received data which is encoded using convolution codes, which has less probability of error compared to other coding techniques. In many digital systems like Viterbi decoder, multiplexers and XOR gates are the major building blocks, which are often designed using transmission gate logic. So, to reduce the power consumption and number of transistors count in the decoder design, the transmission gates are replaced with the pass transistors which contain only one NMOS transistor. Since the eliminated PMOS transistor is large in size, the capacitance in the circuit is reduced thereby reducing the power, size and increase in the speed. This technique is simulated using TANNER tool. The improved performance of Viterbi decoder using pass transistor logic is compared with that of the transmission gate logic and results were compared using TANNER tools.
References

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Index Terms

Computer Science
Circuits And System

Keywords

Viterbi decoder algorithm The branch metric (BM) The path metric Tanner Tools.