Abstract

In this paper, a Novel 16-bit carry select adder (CSLA) is proposed to perform fast arithmetic operation in many data-processing processors. The proposed design combines the modified 16-bit carry select adder and a carry select adder by sharing the common Boolean Logic term. The area and power of the Novel 16-bit carry select adder significantly reduces when compared with modified 16-bit carry select adder[2]. This work evaluates the performance of the proposed design in terms of total number of gates, area, delay and power using Cadence Virtuoso gpdk 180nm technology. In this proposed design the transistor count of a 16-bit carry select adder reduced from 470 to 432 gates which reduce the area by 13.64µm². Moreover, the power consumption has reduced from 9.206n watts to 6.648n watts. The delay of the Novel 16-bit carry select adder increased by 29.626*10^-18s. The result analysis shows that the Novel 16-bit CSLA is better than modified and regular 16-bit CSLA [1].

**Index Terms**

Computer Science

Circuits And Systems

**Keywords**

Carry select adder  Area-efficient  Low power  Hardware sharing  Boolean logic.