Minimizing Power Consumption in CMOS Full Subtractor using SVL Technique

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Abstract

Full Subtractor using Self Controllable Voltage Level (SVL) Technique is designed in this paper. The circuit can supply an increased dc voltage to an active-load circuit required or can decrease the dc voltage supplied to a load circuit under standby mode is developed. Full Subtractor is a consumed low power and low Leakage as compare to conventional design with SVL technique. We may reduce the value of total power dissipation by applying the U-SVL (upper Self Controllable voltage level) technology in which the supply potential is increased and L-SVL (Lower Self Controllable voltage level) technology in which the ground potential is raised. The analysis paper represents how to control power using SVL techniques. The SVL technique based Full Subtractor compared to conventional design that based on power consumption, propagation delay speed and layout area is more preferred. Low-power techniques projected to reduce power in nanoscale CMOS-Very Large Scale Integration (VLSI) systems, Using SVL technique. The result shows that there is significant reduction in Power assimilation of Full Subtractor in reference mode. This design is much useful in designing the system that low power consumed. The circuit is designed using Cadence Tools in 45nm Technology.

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Index Terms

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Keywords

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