Abstract

In this paper a design of 16:1 tree type multiplexer has been presented using GDI and PTL technique. The proposed design consists of 31 NMOS and 15 PMOS. The proposed multiplexer is designed and simulated using DSCH 3.1 and MICROWIND 3.1 on 180nm technology. Performance comparison of proposed multiplexer with CMOS, Pass transistor and transmission gate logic design techniques is also presented. The different logics are compared with respect to Area and Power. A power comparison with respect to supply voltage has been performed using 180nm technology. At 1.2 V power supply the proposed MUX design consumes 56.046 ?W power on BSIM-4 and 56.043 ?W power on LEVEL-3. The proposed design has shown reduction in power consumption by 90%, 55% and 53% as compared to CMOS, TG and PTL techniques respectively on BSIM-4 simulation model. So the proposed multiplexer design has been proven power efficient in comparison with other logic designs.
CMOS Design of Area and Power Efficient Multiplexer using Tree Topology


Index Terms

Computer Science Circuits And Systems

Keywords

CMOS Gate Diffusion Input Multiplexer Pass Transistor Logic Transmission
Gate tree type.