Abstract

This paper propose a verilog implementation of high speed buffer amplifier for reduce the quiescent current consumption a current reuse technique is used in the output stage of the buffer amplifier. The proposed buffer amplifier implemented in a 0.25 µA CMOS technology demonstrate that an average value of 0.1 µA static current. The settling time 0.2% of the final voltage is 2 ns under a 30 KΩ resistance and 30 pF capacitance load. The area of buffer amplifier is 23.123 µm * 78.250 µm.

References

- Chih-Wen Lu, Ping-Yeh Yin, Kuo, Hsuan-Lun, Salvatore Pennisi, 2012, IEEE Conference Publications ISSN 0271-4302 "A Low-Quiescent Current Two Input/Output Buffer Amplifier for LCDs".
Study of High Speed Buffer Amplifier using Microwind

Topology for LCD Driver Applications


Index Terms

Computer Science
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Keywords

Quiescent current, buffer amplifier, CMOS, PMOS, NMOS.