Abstract

This paper proposes a verilog implementation of high-speed buffer amplifier to reduce quiescent current consumption. A current reuse technique is used in the output stage of the buffer amplifier. The proposed buffer amplifier implemented in a 0.25 µA CMOS technology demonstrates an average value of 0.1 µA static current. The settling time 0.2% of the final voltage is 2 ns under a 30 KΩ resistance and 30 pF capacitance load. The area of buffer amplifier is 23.123 µm * 78.250 µm.

References

- Chih-Wen Lu, Ping-Yeh Yin, Kuo, Hsuan-Lun, Salvatore Pennisi, 2012, IEEE Conference Publications ISSN 0271-4302 "A Low-Quiescent Current Two Input/Output Buffer Amplifier for LCDs";
Topology for LCD Driver Applications.
- Chetan D. Parikh, D. Nagchoudhuri, 2011, IEEE Conference Publications, "A 0.7-V Rail-to-Rail Buffer Amplifier with Double-Gate MOSFETs".
- Amrita Shukla, Puran Gour, Braj Bihari Soni, 2013, ISSN : 2230-7109, IJECT Vol. 4, "Implementation of Low-Quiescent Current Two Input/ Output Buffer Amplifier for LCDs Application"

Index Terms

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