Abstract

This paper propose a verilog implementation of high speed buffer amplifier for reduce the quiescent current consumption a current reuse technique is used in the output stage of the buffer amplifier. The proposed buffer amplifier implemented in a 0.25 µA CMOS technology demonstrate that an average value of 0.1 µA static current. The settling time 0.2% of the final voltage is 2 ns under a 30 KΩ resistance and 30 pF capacitance load. The area of buffer amplifier is 23.123 μm * 78.250 μm.

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Index Terms

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Quiescent current buffer amplifier CMOS PMOS NMOS.