Abstract

Power consumption of any circuit is high during test mode than its normal mode of functioning. Different techniques are proposed to reduce the test power. This paper presents the consolidated research work carried to reduce the test power. Usually the power dissipation is due to the sequential and combinational elements presents in the circuit. In this paper we proposed different methodologies and they are at cell level optimization to reduce test power. The structure of the scan flip-flop is modified to reduce the power due to sequential elements and gating techniques are proposed to reduce power duo to combinational elements. The proposed methodologies are implemented on the different ISCAS benchmark circuit and the experimental results were observed. These experimental results showed that our proposed methods reduced the switching power by 44.58-61.97% including the proposed gating technique, area by 30-45% and the test time by 50%.

References

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Techniques for Low Power and Area Optimized VLSI Testing using Novel Scan Flip-Flop

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Index Terms

Computer Science
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Scan flip-flop  Low power test  Shift cycle  Capture cycle