Abstract

Single Electron transistor have high integration density, ultra-low power dissipation, ultra-small size, unique coulomb blockade oscillation characteristics which makes an attractive technology for future low power VLSI/ULSI systems. The Single Electron Transistor have extremely poor driving capabilities so that direct application to practical circuits is a yet almost impossible, to overcome this problem and to investigate the robustness and fastness of the novel design, the hybrid circuits of SET and CMOS are builded. In this work, novel design of SET-CMOS of Half Subtractor and Full Subtractor circuits are designed.
A Novel Design of SET-CMOS Half Subtractor and Full Subtractor

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**Index Terms**

Computer Science  
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**Keywords**

SET-CMOS  hybrid CMOS-SET circuits  SET modeling and simulation