Abstract

Comparators are a basic design module and element in modern digital VLSI design, digital signal processors and data processing application-specific integrated circuits. This paper comprises of design of three different comparators for 2, 4 and 8 bit magnitude comparison. The above said designs are prepared using two different design approaches: Weighted Logic and PTL. The above two design approaches are designed in a way to endow with good quality performance. The performance of these three different comparators in the two design styles has been compared in terms of area and power consumption which are the important parameters that are considered while designing any digital circuit. The schematic are designed and simulated for its behavior using DSCH-3. The layout of simulated circuits are created using Verilog based netlist file which is then simulated in Microwind 3.1 to analyze the performance of comparators for the two design styles at 45nm and 32 nm CMOS technology.

References

Performance Analysis of Magnitude Comparator using Different Design Techniques

- Chiou-Kou Tung; Yu-Cherng Hung; Shao-Hui Shieh; Guo-Shing Huang, &quot;A Low-Power High-speed Hybrid CMOS Full Adder For Embedded System,&quot; IEEE Transaction on Design and Diagnostics of Electronic Circuits and Systems, Vol. 13, No. 6, pp. 1-4, 2007.
- Arkadiy Morgenshtein, Viacheslav Yuzhaninov, Alexey Kovshilovsky, Alexander Fish, &quot;Full-swing Gate Diffusion input logic,&quot; Integration, the VLSI Journal, Vol. 47, pp. 62-70, 2014.
Performance Analysis of Magnitude Comparator using Different Design Techniques


Index Terms

Computer Science Circuits And System

Keywords

ALU Comparators CMOS style Digital Arithmetic Full Adder module PTL logic GDI technique.