Abstract

To design the power and area proficient fast speed data path logic systems, the field of very large scale integration (VLSI) is the generally significant area of research where minimize the area and power is the more difficult task. In digital system, mostly adders lie in the crucial paths that affect the whole performance of the system. To perform the fast arithmetic functions in many data processing processors at low cost, carry select adder is the most suitable adder among the various adders. In this paper, we describe the different techniques which are used to design the proficient CSLA.

References

- I. C. Wey, Y. S. Lin, C. C. Peng and C. C. Ho, "An area-efficient carry select
Different Techniques used for Carry Select Adder - A Review


Index Terms

Computer Science

Circuits And Systems
Keywords
Carry Select Adder (CSLA)  Arithmetic logic unit (ALU)  RCA  BEC  CBL  D-Latch

Basic unit.