Abstract

The synchronizer is constrained such that its state does not change when a latching operation fails. Therefore, any failed latching attempts are automatically retried in the subsequent cycles. For this we simulate the 8 bit multiplier, 4 bit 16 state finite state machine, 16 slot 8 bit data first in first out register etc. In a multi clock system, synchronizers are required when on-chip data cross the clock domain boundaries which guard against synchronization failures but introduce latency in processing the asynchronous input. We use method that hides synchronization latency by overlapping it with computation cycles. Synchronous logic is designed such that state bit transitions have sufficient time to propagate to subsequent flip-flops by the time of the following clock edge. If one flip-flop k becomes metastable and produces a transition whose clock-to-q delays is longer than expected, this transition may not have sufficient time to reach all destination flip-flops.

Index Terms

Computer Science

Circuits And Systems
Keywords

Synchronization failure  Setup time  Holds time  soft error rate  Flip-Flops  Metastability.