Abstract

A large amount of research is currently going on in the field of reversible logic, which have low heat dissipation, low power consumption, which is the main factor to apply reversible in digital VLSI circuit design. This paper introduces reversible gate named as "Inventive0 gate". The novel gate is synthesis the efficient adder modules with minimum garbage output and gate count. The Inventive0 gate capable of implementing a 4-bit ripple carry adder and carry skip adders. It is presented that Inventive0 gate is much more efficient and optimized approach as compared to their existing design, in terms of gate count, garbage outputs and constant inputs. In addition, some popular available reversible gates are implemented in the MOS transistor design the implementation kept in mind for minimum MOS transistor count and are completely reversible in behaviour more precise forward and backward computation.
Lesser architectural complexity show that the novel designs are compact, fast as well as low power.

References


Cost Efficient Design of Reversible Adder Circuits for Low Power Applications


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Keywords
Reversible logic Reversible ripple carry adder Reversible carry skip adder Low power computing.