Abstract

Laboratory testing of digital beamforming processor is required to test and optimize the beamformer algorithm, code and hardware before integrating with antenna and testing the beamformer in an anechoic chamber. Development of a stimulus generator, for carrying out such an exercise, itself can be quite an involved task for a digital beamformer employing a large phased array antenna. This paper proposes an innovative design of a stimulus generator for the receive beamformer system. A reconfigurable hardware prototype, with a Xilinx Virtex-5 FPGA based architecture, is developed to generate IF stimulus for an 8-elements receive beamformer. It can provide a stimulus for up to four transmitting sources, each with programmable frequency, bandwidth, direction of arrival, S/N and interference. The beamformer performance testing for selective element failure can also be facilitated. Testing of
Reconfigurable Stimulus Generator for Receive Beamformer Test-bed

A beamformer with larger phased array antenna can be achieved using multiple cards. The hardware test results are reported.

References

- Heung-Jae Im, Wonsang Hwang, Seungwon Choi, Hyeongdong Kim, "Performance analysis of a smart antenna system utilizing a test-bed implemented on a DSP board," Microwave Conference Asia-Pacific, 2000, pg799 – 803

Index Terms

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