Abstract

The implementation of residue number system reverse converters based on well-known regular and modular parallel prefix adders is analyzed. The VLSI implementation results show a significant delay reduction and area × time² improvements, all this at the cost of higher power consumption, which is the main reason preventing the use of parallel-prefix adders to achieve high-speed reverse converters in recent systems. Hence, to solve the high power consumption problem, novel specific hybrid parallel-prefix based adder components that provide better trade-off between delay and power consumption are herein presented to design reverse converters. We propose Parallel distributed arithmetic convolution technique in Reverse Converter to increase the system performance.

References

- L. Sousa and S. Antão, "MRC-based RNS reverse converters for the four-moduli+?sets \(\{2n + 1, 2n \pm 1, 2n, 22n+1 \pm 1\}\) and \(\{2n+ 1, 2n \pm 22n, 22n 1 1\}\)," IEEE Trans. Circuits Syst. II, vol. 59, no. 4, pp. 244–248, Apr. 2012.
Design and Implementation of RNS Reverse Converter using Parallel Prefix Adders

Index Terms

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Keywords

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parallel distributed arithmetic convolution architecture
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