Abstract

SystemVerilog is the emerging language of choice for modern day VLSI design and verification. SystemVerilog (SV) brings a advanced level of abstraction to the system being modeled. The advanced constructs it utilizes its OOP capability make it stand apart from other verification languages. In this paper we will be analyzing the performance of SV testbench over Verilog testbench, using well defined comparison parameters tested against an actual IP design block, along with other features of the SV language.

References

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Performance Analysis of Verilog Directed Testbench vs Constrained Random SystemVerilog Testbench

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Index Terms
Computer Science Circuits And Systems

Keywords
Assertions Coverage Environment Mailbox Randomization SystemVerilog Threads
Transactions Testbench