Abstract

This paper discusses a rail to rail swing, mixed logic style 1-bit 28-transistor (28T) full-adder, based on a novel architecture. The performance metrics: power, delay, and power delay product (PDP) of the proposed 1-bit adder is compared with other two high performance 1-bit adder architectures reported, till date. The proposed 1-bit adder has a 50% improvement in delay, and 49% improvement in power-delay-product, over the two reported architectures, verified at 90nm technology. The power performance of proposed 1-bit adder and that of the two reported architecture are comparable, within 8%. This analysis has been done at supply voltage VDD = 1.2V, load capacitance CL=150fF, and at a maximum input signal frequency fMAX=200MHz. Also, the worst case performance metrics of the proposed 1-bit adder circuit is seen to be less sensitive to variations in VDD and CL, over a wide range from 0.6V to 1.8V, and from 0fF to 200fF, respectively.
Study of Power-Delay Characteristics of a Mixed-Logic-Style Novel Adder Circuit at 90nm Gate Length


Index Terms

Computer Science

Circuits And Systems

Keywords

Full-adder Mixed logic style 28T 1-bit adder Power delay product Worst-case delay

Worst case power

Carry dependant sum

Input vector transition
and Adder architecture.