Abstract

According to the modern research the rapid development of portable electronics is forcing the designers to elevate the existing designs for better performance. Addition is the crucial arithmetic operation used in various applications like, Digital signal processors, ALUs, math processor and in various other scientific applications. In this paper, we proposed the 1-bit CSA with gates having different values of NMOS & PMOS. Simulation results are presented at 45nm, 90nm and 180nm technologies. The performance parameters like area, power consumption and delay are observed at 45nm, 90nm and 180nm technologies using TANNER tool. In this paper, CSA are examined to study the data dependency and to recognize redundant logic operations. With the help of multiplexer, we can choose accurate output result according to the logic state of input carry signal. In this, we have removed all the redundant logic operations existing in the conventional CSA and suggested an innovative logic formulation for 1-bit CSA. The suggested CSA design comprises significantly less area and delay than in recent times suggested binary to excess-1 converter based CSA.
An Efficient Carry Select Adder Design by using different Technologies

References


Index Terms

Computer Science Circuits And Systems

Keywords

Carry Select Adder (CSA) Arithmetic Unit Low power design SQRT CSA Transmission Gate (TG)
Ripple carry adder (RCA).