Abstract

Digitization of modern world has led to increasing use of digital equipment. The pioneer equipment in this regard is Digital Pulse Width Modulators. Although there is limit on clock frequency which is to be used in digital circuit. This paper describes simple Digital Pulse Width Modulator with optimized Area using Field Programmable Gate Arrays (FPGA). The proposed architecture uses a phase shifter mechanism provided by on chip Digital Clock Manager (DCM) in FPGA. The circuit uses such design to reduce cell Area to greater limit. The design is experimentally tested and compared with other design.

References

Conference and Exposition, Professional Education Seminars Workbook, 2008


Index Terms

Computer Science

Signal Processing

Keywords

HRDPWM, DCM, FPGA, RESET logic