A Review of VLSI Structure for the Implementation of Matrix Multiplication

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Abstract

Matrix multiplication is the kernel operation used in many transform, image processing and digital signal processing application. In this paper, we have studied for parallel-parallel input and single output (PPI-SO), parallel-parallel input and multiple output (PPI-MO) and parallel-parallel fixed input and multiple output (PFI-MO) matrix-matrix multiplication. It is also a well-known fact that the multiplier and adder unit forms an integral part of matrix multiplication. Due to this regard, high speed multiplier and adder become the need of the day. In this paper, we have studied of Vedic mathematics multiplier using compressors.

References

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Index Terms

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Keywords

Parallel-Parallel Input and Single Output (PPI-SO), Parallel-Parallel Input and Multiple Output (PPI-MO), Matrix Multiplication (MM)