Abstract

Reed-Solomon (RS) codes are commonly used in the digital communication. It has high capability to eliminate both random errors and burst errors. In this work, the encoding of RS(255, 223) code is designed, synthesized, and simulated using Verilog language with the device family of virtex4 & device of xc4vfx12 & compare the result with device family Spartan3E & device XC3S100E. During the transfer of message, the data might get corrupted due to lots of disturbances in the communication channel. So it is necessary for the decoder tool to also have a function of correcting the error that might occur. So, from syndrome input-output waveform, it has been checked that whether there is any error in the received codeword or not. RS codes are type of burst error detecting codes which has got many applications due to its burst error detection and correction nature. This code is defined over a Galois Field GF(28) and has the capability of correcting up to sixteen short bursts of errors.
Design and Implementation of RS (255, 223) Detecting Code in FPGA

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Index Terms

Computer Science  Circuits and Systems

Keywords

Reed-Solomon code, Linear Feedback Shift Register, Galois Field, Generator Polynomial, Encoder, Constant Multiplier, Syndrome, Verilog language.