Abstract

Reduction in leakage power has become an important concern in low-voltage, low-power, and high-performance applications. In this paper, the dual-threshold technique is used to reduce leakage power in a 32-bit ripple carry adder by assigning high-threshold voltage to some transistors in noncritical paths, and using low-threshold transistors in critical path. The circuit was implemented using Cadence Virtuoso tools in 90-nm technology. The optimized layout of the ripple carry adder is designed using Cadence Virtuoso Layout Suite. Performance parameters such as total power, delay, static power and power delay product (PDP), were calculated and compared with the existing design topologies of full adder. The simulation results of the 32-bit ripple carry adder using the dual threshold voltage technique are compared with the conventional 32-bit ripple carry adder with different threshold values. Results show that the dual-threshold technique is good for leakage power reduction during runtime mode.

References

**Index Terms**

Computer Science       Circuits and Systems

**Keywords**

Leakage power, static power