Abstract

Shrinking technology enables designers to integrate more functionality with improved performance and density in ICs; but this improvement comes at cost. The impacts of parasitic are dominating circuit performance with leading edge of technology. This paper first presents the post-layout challenges facing by the designers at advanced technology node and then discusses the different advanced techniques used to mitigate those challenges. We can bucket these post-layout challenges mainly in two categories; first “PARASITC EXTRACTION related challenges” and second “POST-LAYOUT SIMULATION related challenges” which includes accuracy, run time and memory usage uses issues. They are causing negative impact on product yield and time-to-market constraint. Finally we conclude this paper by comparing different-different methodologies used for parasitic extraction and simulation.

In summary, In this paper we will discuss the advanced techniques used for the Parasitic extraction and Simulation for the successful tape-out.
References

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Index Terms

Computer Science
Information Sciences

Keywords

Parasitic extraction, Post-layout Simulation, Interconnect Resistance, Interconnect Capacitance, Extracted netlist.