Abstract

In this paper we propose a method for synthesis of combinational networks using non conventional logic gates. The logic components considered are Stochastic Logic Gates (SLGs) able to change their logic functionality by means of a single control parameter and the environmental level of noise. SLGs are able to adapt their computed logic function depending on the environmental conditions. Circuits composed of SLGs are thus sensitive to changes in the environment which alter the computed logic function. We propose a solution for the synthesis of SLGs combinational networks able to produce a network operating fault tolerant in different environmental conditions, i.e. different levels of noise. Given a description of the problem, in form of a truth table, the synthesis of the network is performed by means of genetic algorithms. The proposed solution is tested with a half-adder and compared to the optimal solution found with an exhaustive search.

References


Noise Tolerant Stochastic Logic Gate Circuits Synthesis using Genetic Algorithms


Index Terms

Computer Science
Algorithms

Keywords

Stochastic Logic Gate, Fault Tolerant, Genetic Algorithm, Non Conventional Computing