Abstract

FinFET is a non planar modeling device for small size transistors (less than 45nm) will replace traditional planar MOSFETs because of superior ability to control short channel effects, off-state leakage current, power dissipation and propagation delay. Static random access memories (SRAMs) consume nearly 94% of chip area in most present system-on-chip (SoC) circuits. In this paper, a standard 6T SRAM cell has been designed using dual gate FinFET transistors and its performance for read/write operation is analyzed in terms of average power consumption, propagation delay, power delay product (PDP) and static noise margin (SNM) for nanoscaled technologies. A comprehensive comparison is carried out with conventional 6T CMOS SRAM cell for 45nm, 32nm and 16nm nanoscaled technologies. A reduction in power delay product by 87.5%, 88.8% and 99.1% in read operation and 90.4%, 89.2% and 96.9% in write operation of FinFET based SRAM cell at 45nm, 32nm and 16nm technology nodes respectively as compared to 6T CMOS SRAM cell. Also an improvement in static noise margin by 27.5%, 31.5% and 8.9% of FinFET based SRAM cell is obtained at 45nm, 32nm and 16nm technology nodes respectively.
References

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Index Terms

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Keywords

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