VHDL Implementation of Fast Multiplier based on Vedic Mathematic using Modified Square Root Carry Select Adder

Abstract

In this paper, a novel technique for multiplication is presented using Vedic multiplier. Vedic multiplier uses adders and hence making fast adder will increase the overall speed for multiplication. We have done comparative analysis for multiplication using different architectures of adder. For comparison we have taken Carry Select Adder (CSA), Square Root Carry Select Adder (SQRT-CSA). We have proposed Vedic multiplication using Modified SQRT-CSA. VHDL design is proposed and synthesis is performed on Virtex-4 FPGA.

References

VHDL Implementation of Fast Multiplier based on Vedic Mathematic using Modified Square Root Carry Select Adder


Index Terms

Computer Science

Circuits and Systems

Keywords

Vedic Multiplier, CSA, SQRT-CSA, Modified SQRT-CSA, Binary-to Excess One (BEC) block