Abstract

Scaling in Silicon technology, usage of SRAM Cells has been increased to large extent while designing the embedded Cache and system on-chips in CMOS technology. Power consumption, packing density and the speed are the major factors of concern for designing a chip. The consumption of power and speed of SRAMs are some important issues among a number of factors that provides a solution which describes multiple designs that minimize the consumption of power and this review article is also based on that. This article presents the simulation of 6T, 9T, LP10T, ST10T and WRE8T SRAM cells. All the simulations have been carried out on 90nm at Microwind EDA tool.

References

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**Index Terms**

Computer Science

Circuits and Systems

**Keywords**

Cache Memory, CMOS, Hold Power, Speed.