Abstract

While designing Fast Fourier Transform (FFT) cores, due to the use of multiplexers, memory, or ROMs, there is a substantial increase in power consumption and area. In order to increase speed and throughput, folding and pipelining methods have been approached by various existing designs. But the prime disadvantage of those architectures is the use of multipliers for twiddle multiplications. This present work has proposed fast fourier transform using compressors based multiplier. Both parallel and pipelining techniques have also been used in the proposed designs.

Carry Select adder is known to be the fastest adder among the Conventional adder structures. This work uses an efficient Carry select adder by sharing the binary to excess-1 converter (BEC) term. After a logic simplification, we only need one XOR gate, one AND gate and one inverter gate for carry and summation operation. Through the multiplexer, we can select the correct output according to the logic states of the carry in signal. These all design and experiments were carried out on a Xilinx 14.1i Spartan 3e device family.
FFT utilizing Modified SQRT CSLA and Proposed 5:3 & 9:4 Compressor

References


14. Figure 9: Output Waveform of Proposed Design

Index Terms
Computer Science
Circuits and Systems

Keywords
Fast Fourier Transform (FFT), Regular 16-bit SQRT CSLA, Modified SQRT CSLA
FFT utilizing Modified SQRT CSLA and Proposed 5:3 & 9:4 Compressor