Abstract

The branch predictor plays a crucial role in the achievement of effective performance in microprocessors with pipelined architectures. This paper analyzes performance of branch prediction unit for pipelined processors. A memory of 512 bytes is designed for storing instructions. A 32 byte memory is designed for branch target buffer (BTB). This memory is utilized for storing history of the branch instructions. A Finite State Machine (FSM) is designed for branch predictor unit. It consists of four states: strongly taken, weakly taken, weakly not taken and strongly not taken. Prediction is done based on the status of FSM. If the state of FSM is weakly taken or strongly taken, then predictor guesses it as a taken condition else it is assumed to be not taken condition. When the execution of branch instruction is done for the first time the BTB stores the address of current instruction and also the address where it jumps. After this the current status of the FSM is updated accordingly. The program is executed using a branch predictor unit and also without a branch predictor unit. The latency of both the processors with a branch prediction unit and without is branch prediction unit is computed and compared. The simulation results validates that with branch prediction unit latency is decreased.
References


Index Terms

Computer Science
Circuits and Systems

Keywords

BTB, FSM, ILP, FPGA, Latency, Processor.