Abstract

Transposition memory (TRAM) is one of the most important matrix processing block. This paper presents the design of a transposition memory implemented using 1V 45nm CMOS technology in Cadence® Virtuoso® Design Environment. A new double edge triggered flip-flop based on clock-gated pulse suppression technique is developed. This new double edge triggered flip-flop evolved from clock-gating pulse suppression technique reduces the power dissipation in the clocking system. This new clock-gated pulse suppressed double edge triggered flip-flop (CGPSDFF) is used to design the D flip-flop based architecture of a high speed TRAM and power reduction of the CGPSDFF-based TRAM is 20% better than conventional TRAM.

References

Innovative Low Power Transposition Memory using Double Edge Triggered Flip-flop

MP@ML exploiting data distribution properties for minimal activity, ” IEEE J. Solid-State Circuits, vol. 34, no. 5, pp. 693-703, May 1999.


Index Terms
Keywords

Low power, TRAM, clock system, clock-gated pulse suppression technique, CGPSDFF