Performance Analysis of Full Adder Circuit using Double Gate MOSFET

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Abstract

This paper presents a design of a one bit full adder cell based on stack effect using Double Gate MOSFET. This design has been compared with existing one-bit full adder which is designed using power gating technique. In this paper, the proposed circuit has been analyzed for parameters like- power consumption and power delay product. The simulations of the proposed Full Adder have been performed using Tanner EDA Tool version 13.0. All the proposed design simulations are carried out at 45nm technology for various inputs like supply voltage and input voltage. The decrease of 99.5% in power utilization has observed in proposed circuit. The results show a legality of double gate MOSFETs for designing for low power full adder circuit.

References

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Index Terms

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Keywords

Full Adder; Stack effect; Double Gate; Low Power; PDP ; power gating