Abstract

Routing of arbitrary placed blocks has been a long prevailing objective in any circuit in VLSI. In FPGA, the routing problem becomes more complex due to its fixed routing resources. An efficient routing algorithm tries to reduce the lengths of critical-path nets and also the congestion in the channel to improve the performance of the circuit. This paper presents an Ant System based approach, based on the intelligent behavior of ants, for the routing problem in FPGA. It is observed that the results after some iterations, converge towards the optimal solution at a better rate than other comparable techniques.
Ant System for Routing in FPGA


**Index Terms**

Computer Science

Networks

**Keywords**

Field Programmable Gate Array (FPGA), Application Specific Integrated Circuits (ASIC), Routing, Ant Colony Optimization (ACO).