Review of SOI MOSFET Design and Fabrication Parameters and its Electrical Characteristics

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Abstract

In current scenario the device count in an IC is running into billions per chip, the issue of power dissipation in the chip is becoming too critical. Due to decreasing device dimension the performance of the bulk Si MOSFET is limited by its fundamental physical limitation like reduction in carrier mobility due to impurities, p-n junction leakage current increases as the junction become more and more shallow and increasing gate tunneling effect as the gate oxide thickness decreases. These requirements have led to development of alternating technology. SOI (silicon on insulator) technology is an alternative choice of Conventional Technology which offers the performance as may be expected from the next generation technology. SOI technology offers significant advantages in fabrication, design and performance for many semiconductor circuits such as excellent isolation, radiation hardness, improved latch up free operation, reduced short channel effects, improved switching speeds and reduced leakage current, due to reduction in the drain-body capacitance. The reduction in the parasitic capacitances provides improved switching speed and superior performance. This paper is focused on the brief of SOI MOSFET Technology, its characteristics, advantages and
disadvantages of it.

References


Proceedings of the IEEE SOI Conference, October 5-8, Stuart, Florida, USA.


**Index Terms**

Computer Science

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**Keywords**

SOI, MOSFET, CMOS, wafer, Silicon, Insulator