Abstract

Error detection is the detection of errors caused by noise or other impairments during the transmission of signal from transmitter to receiver. Logic design errors may occur during simulation and synthesis due to increase in the complexity of CMOS and VLSI circuits. Error detection method can be either systematic or non-systematic. In systematic method, the transmitter sends the original data unit, and a fixed number of check bits or Parity data is been attached to it, which are derived from the same input data unit. In this work, we describe a method of error detection in 4-bit multiplier with parity predictor circuit in QCA tool. 4-bit multiplier is used as a logic in which we detect error according to its input data. The outputs of logic used and the parity predictor are then compared using comparator. If the values do not match, error has occurred. The technique we used is Concurrent error detection using parity predictor circuit.
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Index Terms

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Error Detection, Systematic scheme, Parity predictor, Comparator, Concurrent Error Detection.