Abstract

Error detection is the detection of errors caused by noise or other impairments during the transmission of signal from transmitter to receiver. Logic design errors may occur during simulation and synthesis due to increase in the complexity of CMOS and VLSI circuits. Error detection method can be either systematic or non-systematic. In systematic method, the transmitter sends the original data unit, and a fixed number of check bits or Parity data is been attached to it, which are derived from the same input data unit. In this work, we describe a method of error detection in 4-bit multiplier with parity predictor circuit in QCA tool. 4-bit multiplier is used as a logic in which we detect error according to its input data. The outputs of logic used and the parity predictor are then compared using comparator. If the values do not match, error has occurred. The technique we used is Concurrent error detection using parity predictor circuit.

References
Error Detection in 2-bit & 4-bit Multiplier using Parity Predictor Circuit in QCA

1. Prof. John Kimani “A Combinational Multiplier Using the Xilinx Spartan II FPGA”, Northeastern University, EECE 2160.

2. Ms. R.S.Khond1, Prof.P.R.Indurkar2, Prof. P.R Lakhe3 “REVIEW ON DIFFERENT ERROR CORRECTION CODES”, 1Department of Electronics Engineering S.D. College Of Engg. 2Department of ENTC B.D. College Of Engg..3 Department of Electronics Engineering S.D. College of Engineering Wardha, Maharashtra, India


8. Dr. E. N. Ganesh 2010 "Implementation and simulation of arithmetic logic unit, shifter and Multiplier in Quantum Cellular automata technology.", (IJCSE) International Journal on Computer Science and Engineering Vol. 02, No. 05.


10. Ismo H"anninen and Jarmo Takala, December 2007 "Binary Multipliers on Quantum-Dot Cellular Automata", FACTA UNIVERSITATIS (NIŠ)SER: ELEC. ENERG. vol. 20, no. 3.

11. Subhasish Mitra and Edward J. McCluskey “WHICH CONCURRENT ERROR DETECTION SCHEME TO CHOOSE?”


Index Terms

Computer Science

Circuits and Systems

Keywords
Error Detection, Systematic scheme, Parity predictor, Comparator, Concurrent Error Detection.