Abstract

The proposed buffer achieves low offset and high slew rate in proposed circuit NMOS folded cascode operation amplifier is used instead of rail to rail operation amplifier, use of only NMOS folded cascode operation amplifier reduces the number of MOS used in circuit and using auto zero negative feedback will provide full swing for positive and negative feedback polarity pixel, and to decrease the offset a current distributed load is used which increases DC gain of operational amplifier and as DC gain increases it reduces offset voltage and increases slew rate with same bias current used in folded and summing stage of operational amplifier. The proposed circuit is simulated and verified in LT-spice and Microwind simulation tool using 350nm CMOS TSMC foundry with 3.3 V supply voltage the offset calculated is around .2mV and slew rate is 14V/µs.

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Index Terms

Computer Science
Circuits and Systems

Keywords

LCA, Buffer Amplifier