Implementation of a Single-Channel HDLC Controller on FPGA

Abstract

HDLC are the high level data link control procedures established by ISO. They are widely used in digital communication and are the bases of many other data link control protocols. The objective of this paper is to implement a Single-Channel HDLC Controller on an Altera FPGA. All the modules such as the transmitter and the receiver are designed and implemented using VHDL programming language and illustrated with a detailed schema. The software tools used in this work include Altera Quartus II 8.1 and ModelSim Altera 6.1g. The target circuit is the Cyclone II EP2C35F672C6.

References

2. Yuanlin Lu; Zhigong Wang; Lufeng Qiao; Bin Huang, "Design and implementation of multi-channel high speed HDLC data processor," in Communications, Circuits and Systems and
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Index Terms

Computer Science  Signal Processing
Keywords

HDLC, Data Link Control Layer, Altera FPGA, bit stuffing/unstuffing, CRC-16, CRC-32, Flag.