Area Efficient High Speed Vedic Multiplier using Common Boolean Logic

Abstract-In the advanced digital technology the need is of high speed in real time system along with the improvement in implementation issue. Vedic Multipliers has been used to solve the typical and tedious engineering calculation by simple Vedic methods. Here in this paper we have proposed the Vedic multiplier with Common Boolean Logic adder to improve the propagation delay time and area on silicon chip. With this slight improve in the multiplier, great results have been achieved in signal processing tasks. The VM has been designed for the target device XC3S400 -5 PQ208.

References


Index Terms

Computer Science

Circuits and Systems

Keywords

FIR filters, Common Boolean Logic (CBL), Vedic Multiplier, Digital Signal Processing.