An Enhanced Secured FPGA based DES

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Abstract

In this paper we demonstrate an efficient and compact reconfigurable hardware implementation of the Data Encryption Standard (DES) algorithm. Our design was implemented on FPGA of device VirtexEXCV400e. As a strategy to reduce the associated design critical path, we utilized a parallel structure that allowed us to compute all the eight DES S-boxes simultaneously. The testing of the implemented design shows that it is possible to generate data in 16 clock cycles when non-pipelined approach is employed. When pipelined approach is employed on the other hand, 17 clocksignals are required for the initial phase only, and one clocksignal is sufficient afterwards for each data generation cycle. The Very High Speed Integrated Circuit Hardware Description Language (VHDL) is used to program the design.

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Index Terms

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Keywords

DES, FPGA, Parallel structure.