Abstract

In this paper we will do the analysis of the gate engineering impact on tri state inverter performance for the application on SOC that is system on chip with the help of different high dielectric material. The high dielectric materials used in electronic circuits for preventing tunnelling effect which will increase the thermally generated current. In order to reduce the Thermally generated current occurs in electronic circuit we can replace the sio2 with different materials having high dielectric constant. Tri State Inverter is designed by the use of microwind tool or simulator. The performance of Device is analysed for various parameter. It is measured that by the use of high dielectric constant material in Tri State Inverter the thermally generated current and dissipation of power minimised and also the performance of the circuit gets high. Among various high dielectric constant material, Lanthanum oxide La2o3 gained focus due to its property such as High Energy Band Gap, High Dielectric Constant, and can resist up to high Temperature.

References
12. Nirmal 1, Divyamarythomas 3, Shruti.k 4 and Patrickchella Samuel“ Impact of Gate Engineering on Double Gate MOSFET using High-k Dielectrics” IEEE 2011.

Index Terms

Computer Science
Power Electronics

Keywords

Tri State Inverter, Low Power, High k, CMOS, VLSI, TG Current.