Digital signal processing typically requires large number of mathematical operations to be performed repeatedly on the samples of data with less delay and power consumption. Multiplication is the fundamental arithmetic operation and determines the overall execution time of the processor. In this paper two high speed 32-bit Vedic multipliers are designed based on Urdhva-Triyakhbhyam sutra. Addition of partial products of proposed multipliers is done using Kogge stone adder and ripple carry adder respectively. Proposed multiplier-1 and proposed multiplier-2 were compared with the one with the highest speed and a reduction of 77% and 65.37% is achieved respectively. The coding is done using Verilog HDL and synthesized using cadence tool.

References


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Index Terms

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Vedic Mathematics, Urdhva Triyakhbhyam, Kogge Stone Adder, High Speed.