Abstract

A greater part of the low power design methodology is allocated for reducing leakage current. This plays a vital role in static power dissipation. In this project, a current comparison domino pull-up network with its worst case leakage current is compared with Current comparison based Domino (CCD) with Clamped bit-line Current-sensing Amplifier circuit. Thus, the contention current and consequently power consumption and delay are reduced. The leakage current is also decreased by utilizing the footer transistor in diode configuration, which results in increased noise immunity. The simulation results of wide fan-in gates designed using a 16-nm high-performance predictive technology model demonstrates 46% power reduction and at least 2.36× noise-immunity improvement at the same delay compared to the standard domino circuits for wide fan – in OR gates.

References

Leakage High-Speed Domino Circuit for Wide Fan-In Gates”, IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS.


**Index Terms**

Computer Science \hspace{5cm} Power Electronics

**Keywords**

Clamped bit-line Current Sense Amplifier, Domino Logic.