Abstract

This paper presents a differential architecture of CMOS transimpedance amplifier offered to obtain the input capacitive load insensitive and the very minimum noise structure. The suggested TIA is dependent on the differential structure and composed of a regulated cascode block and a differential amplifier along with active feedback. To increase the bandwidth of the amplifier series inductive peaking and a capacitive degeneration step employed. Simulation results shows that the TIA achieves 100 GHz bandwidth, 80.4 dBΩ transimpedance gain, and 20 pA/

References

Design of CMOS based Transimpedance Amplifier for Bandwidth Enhancement with Large Gain

2010.


4. Maruf N. Ahmed, Joseph Chong, and Dong Sam Ha “ A 100 GB/s Transimpedance Amplifier in 65 nm CMOS Technology for Optical Communications” Multifunctional Integrated Circuits and Systems..

5. Dandan Chen, Kiat Seng Yeo, Senior Member, IEEE, Xiaomeng Shi, Manh Anh Do, Senior Member, IEEE Chirn Chye Boon Senior Member, IEEE, and Wei Meng Lim, “Cross-Coupled Current Conveyor Based CMOS Transimpedance Amplifier for Broadband Data Transmission” IEEE transactions on very large scale integration (vlsi) systems, vol. 21, no. 8, august 2013.


15. Omeed Momeni, Student Member, IEEE, Hossein Hashemi, Member, IEEE, and Ehsan Afshari, Member, IEEE A 10-Gb/s Inductorless Transimpedance Amplifier IEEE transactions on circuits and systems—II: express briefs, vol. 57, no. 12, december 2010


Index Terms

Computer Science

Circuits and Systems

Keywords

CMOS, Inductive series peaking, Transimpedance amplifier (TIA), Bandwidth enhancement, RGC, Capacitive degeneration, Active feedback.