Abstract

This paper presents a differential architecture of CMOS transimpedance amplifier designed to obtain the input capacitive load insensitive and the very minimum noise structure. The proposed TIA is based on a differential structure and composed of a regulated cascode block and a differential amplifier along with active feedback. To increase the bandwidth of the amplifier, a series inductive peaking and a capacitive degeneration step are employed. Simulation results show that the TIA achieves 100 GHz bandwidth, 80.4 dBΩ transimpedance gain, and 20 pA/
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Index Terms

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Keywords

CMOS, Inductive series peaking, Transimpedance amplifier (TIA), Bandwidth enhancement, RGC, Capacitive degeneration, Active feedback.