Abstract

This paper presents a differential architecture of CMOS transimpedance amplifier designed to achieve input capacitive load insensitivity and very low noise structure. The suggested TIA is based on a differential structure and comprises a regulated cascode block and a differential amplifier along with active feedback. To increase the bandwidth of the amplifier, series inductive peaking and a capacitive degeneration step are employed. Simulation results show that the TIA achieves 100 GHz bandwidth, 80.4 dBΩ transimpedance gain, and 20 pA/

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Design of CMOS based Transimpedance Amplifier for Bandwidth Enhancement with Large Gain


Index Terms

Computer Science Circuits and Systems

Keywords

CMOS, Inductive series peaking, Transimpedance amplifier (TIA), Bandwidth enhancement, RGC, Capacitive degeneration, Active feedback.