A Survey Paper on Implementing MTCMOS Technique in Full Subtractor Circuit

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Abstract

This paper presents the study and survey analysis of Full Subtractor circuit on implementing the MTCMOS technique. Full Subtractor is a combinational circuit that performs subtraction and results in difference and borrows outputs. Implementing the MTCMOS technique on this circuit results in reduction of both leakage current and power consumption.

References

2. Basha MM., Dr. Ramanaiah KV, Dr. Reddy PR, “Novel energy efficient 1-bit full subtractor at 65nm technology” Electrical, Electronics, Signals, Communication and Optimization (EESCO), 2015.


**Index Terms**

Computer Science  
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**Keywords**

Full Subtractor, MTCMOS, leakage current, power dissipation.