Low Power and High Speed 13T SRAM Cell with Bit-Interleaving Capability

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ABSTRACT
In this paper a low power single ended 13T SRAM cell has been proposed for bit inter-leaving application. A column aware scheme is used in the cell to achieve stable SRAM cell with better performance than the existing designs. The proposed SRAM cell exhibit robust read operation and better read performance with lower power consumption. This proposed 13T SRAM has been compared with standard 6T SRAM and existing 9T SRAM (with bit-interleaving capability) in term of Power consumption, Delay and Power Delay Product (PDP) at various supply voltages as 1.8V, 1.6V and 1.4V. The simulations are carried out on Cadence Virtuoso at 180nm CMOS technology and the simulation results are analyzed to verify the superiority of the proposed design over the existing designs. The proposed 13T SRAM proves to be better in terms of power and PDP at all the supply voltages. At 1.8V power saving by the proposed circuit is 72.46% compared to standard 6T SRAM cell and significant improvement is observed at other supply voltages also.

Keywords
SRAM cell, Leakage Power, Low Power, Stability, Bit-interleaving, PDP.

1. INTRODUCTION
Static Random Access Memory (SRAM) is an important part of the microprocessor world, but for the DSM (deep submicron tech) circuit as the size of the CMOS is scaling down; the leakage current is most common problems for SRAM cell, which is basically designed for very low power application. Consequently, In SRAM power consumption becomes a major issue and low power design of SRAM without compromising with the speed performance becomes major concern in modern very large scale integration (VLSI) designs. Furthermore due to scaling the circuits face design challenges for nanometer SRAM design. Because of low V_{th} and ultra-thin gate oxide, the leakage power consumption is increased [1]. The stability during read and write also affected [2]. The adoption of supply voltage scaling proves to be most effective in energy saving since it can reduce the power of thecircuit in significant amount [3]. But with the miniaturization of devices and supply voltage scaling, the variability of SRAMs in process parameters and threshold voltage together with I_{on}–I_{off} ratio increase severely and this degrades the Static Noise Margin (SNM) drastically [4, 5]. Furthermore, the SNMs are linearly dependent on the supply voltage, as the supply voltage is scaled down to save power the cell stability severely get affected. Hence obtaining ultra-low power consumption while maintaining the cell stability becomes the main motive of SRAM designs in this scenario. Voltage reduction along with device scaling is associated with decreasing signal charge. In this paper, a 13T SRAM cell has proposed with bit-interleaving capability with better performance. Some other SRAM cell with bit interleaving have been presented in [6-10] in past. The proposed design has less power consumption, high speed, improved write ability, read robustness.

The brief overview of this paper as follows, in section 2 literature review i.e. standard 6T SRAM and existing 9T SRAM cell for bit-interleaving capability has been discussed. Section 3 consists of elaboration of the proposed work, section 4 contains the simulation and results discussion and section 5 consists of conclusion part.

2. LITERATURE REVIEW
2.1 Standard 6T SRAM Cell
Standard 6T SRAM cell consists of two back to back connected cross coupled inverters (N1 P1, N2 P2), two access NMOS transistors N3 and N4 acting as pass transistors and two data storing nodes (Q and QB) which the pass transistor N3 and N4 are access by as shown in Fig.1. These cross-coupled inverters forming the latch, i.e. each bit is stored in the latch. The access transistors are enabled using Word Line (WL). When the Word Line (WL) is low, access transistors are disabled and cell works in hold state, at this time read or write operations cannot be performed, at this state latch can hold bit as long as the voltages remain at V_{dd} and GND. When the word line becomes high, access transistors N3 and N4 are enabled, and at this stage read and write operations can be performed [5]. Data is write at node Q through bit line and opposite data is stored at the node QB.

The 6T SRAM cell is used shared word-line architecture though this technique is simple and commonly used to arrange array of cell. The main disadvantage of this architecture is that the multi-bit soft error is very high since the adjacent bit share a WL each other. Apart from this 6T SRAM cell has read failure which is overcome in [11], write 1 failure [12] and also consume more power.

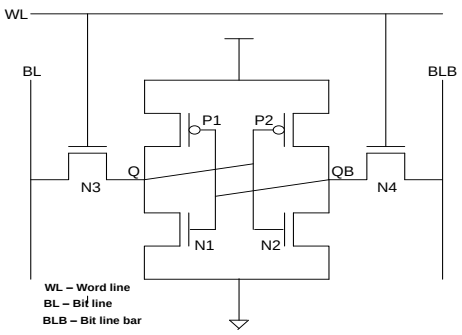


Fig 1: Standard 6T SRAM cell

2.2 Existing 9T SRAM cell

In 9T SRAM cell three extra transistors N5, N6, P3 are added. Transistor N5 is connected between node Q and N1 for the data protection during read operation [11] , this transistor prevent the discharging of node Q since it turn off during read , write operation . Transistor (N6, P3) forms a special inverter for AND logic operation [10] to activate local word line (LWL). It also have bit line (BL) ,world line (WL) and provide extra word line (RWL) for read operation , bit line CBLB to control transistor N5 as shown in Fig. 2 . This 9T SRAM cell is designed with bit interleaving capability for soft error protection and this design also sort-out the problem of write 1 failure which was occurring in 6T SRAM cell. Also exhibit considerable improvement in write ability, read robustness, lower write and leakage power consumption, as well as has better tolerance in process variation [12]. Still average power and speed of the circuit can be further improved by connecting some extra transistor which is done in the proposed 13T circuit.

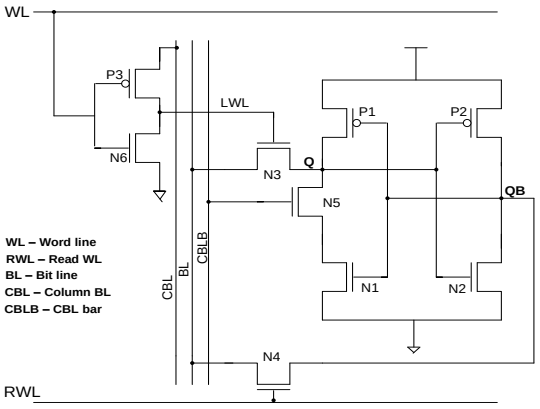


Fig 2: 9T SARM cell

3. PROPOSED WORK

3.1 Proposed 13T SRAM Cell

Single ended 13T SRAM cell for bit interleaving application has been proposed, the bit interleaving idea originate from the differential 8T SRAM cell [10]. Subsequently this idea is used in read disturb free 9T SRAM cell [12]. The working of the proposed cell is similar to the 9T SRAM cell with less power consumption, high speed, less PDP. In the schematic we have connected four extra transistor three NMOS (N7, N8, N9) and one PMOS (P4) as shown in Fig. 3. Two NMOS (N7 & N8) are stacked with the transistor N1 and N2 that increases the threshold voltage V_{th} to reduce sub- threshold leakage current and consequently leakage power will be reduced [13]. Apart from this, two sleep transistor PMOS (P4) , NMOS (N9) also connected with pull up (P1 and P2) and pull-down (N7 and N8) networks respectively as shown in Fig.3. In this circuit, in the active mode, both the sleep transistors (P4 and N9) are turned 'ON'. So, P4 passes full supply swing V_{dd} and N9 passes full ground voltage (‘0’).

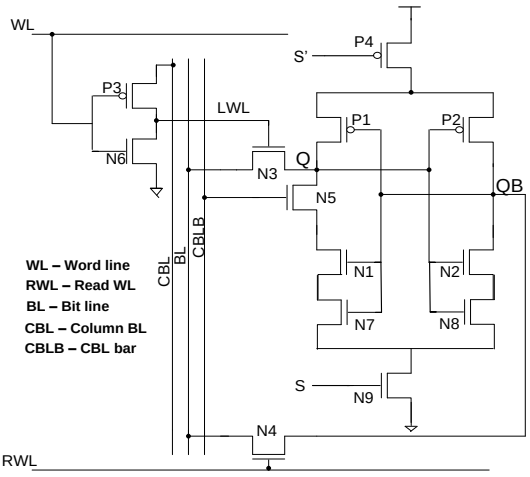


Fig 3: Proposed 13T SRAM cell

In the stand-by mode both transistors PMOS (P4) and NMOS (N9) are in 'OFF' state and leakage is reduced. The operation principle of our proposed 13T SRAM cell is discussed below.

Hold mode:

In hold mode, set the word line (WL) at high voltage while RWL signal switch low, hence transistor N3 & N4 turn off to prevent the access of bit line, CBLB is set high to turn on transistor N5 as a result data retention is afforded by the cross coupled back-to- back pair .

Write Mode:

In write operation pull down WL at low and enable CBL signal, then LWL signal is pre-charged to high value as a result the data is written from bit-line (BL) to storage nodes (Q & QB) through N3 .

Read mode:

During read mode first of all BL is set to high , then the special read word line (RWL) signal start read operation , CBL turns high and the CBLB is turn to low voltage and WL remains at high .

From simulation result it is observed that proposed 13T SRAM cell generates Q and QB output which has proper logic without delegation of output waveform. The output waveform for proposed 13T SRAM cell is shown in Fig. 4.

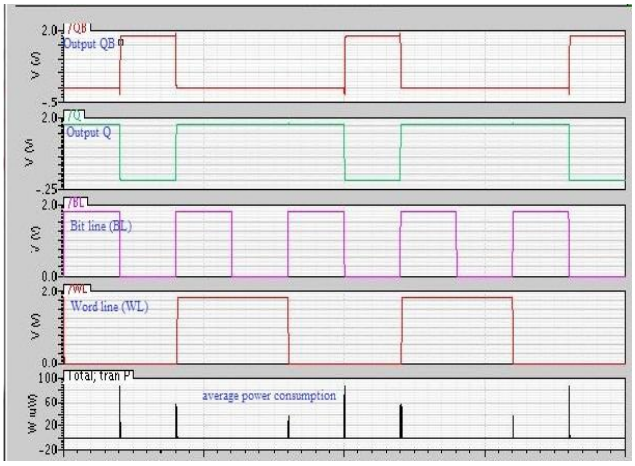


Fig 4: Output Waveform of Proposed Circuit

3.2 Bit-Interleaving And Shared Word Line Architectures

Mainly two ways are used to arrange the words in SRAM architecture. Shared word line shown in Fig. 5(a) and bit interleaving shown in Fig. 5(b). In the share word line architecture, all the bits of the same words are located next to each other clearly shown in figure. This design is widely used because of its simplicity and compactness, since bits are adjacent to each other, the probability of multi-bit soft errors is very high. To solve the problem of soft errors bit interleaving architecture is used. A detailed explanation of these techniques is given in [10]. Bit-interleaving is commonly used in SRAM design, to provide soft error protection as well as area efficient utilization of wiring.

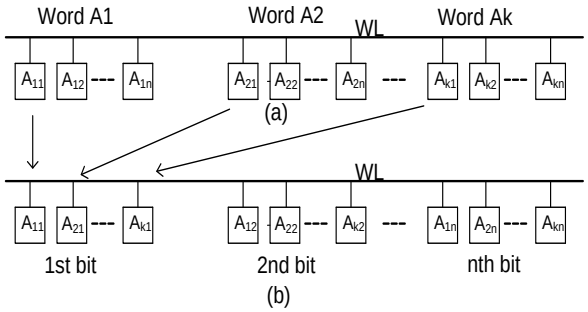


Fig 5: SRAM word organization (a) Shared word line (b) Bit-interleaving

Fig. 6 shows 2x2 bit-interleaving architecture of proposed 13T SRAM cell. The detail explanations and the working of 2x2 bit-interleaving architecture is given in [12].

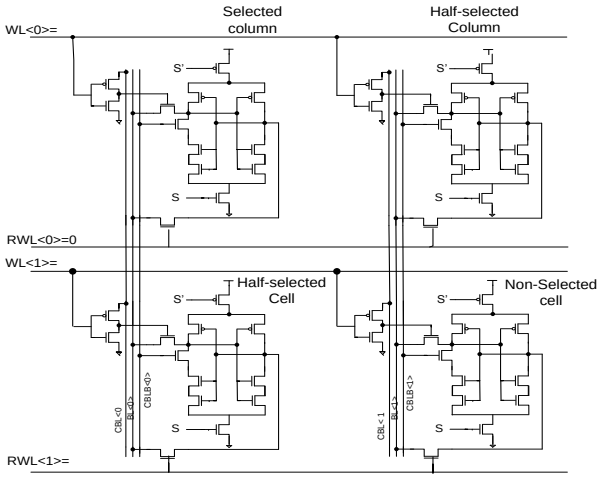


Fig 6: The 2x2 bit-interleaving architecture of 13T SRAM cell.

4. SIMULATION AND RESULT DISCUSSION

All the existing and proposed circuit is simulated in Cadence Virtuoso at 180nm technology at frequency 25 MHz Power consumption and delay is calculated at various supply voltages 1.8V, 1.6V and 1.4V respectively. It is observed that as we scale down the supply voltage the power consumption of the SRAM cell also reduces. The size (W/L ratio) of the transistors (N-CMOS and P-CMOS respectively) is taken to be the same for all transistor of the cell to compare different type of SRAM cell. The proposed SRAM cell shows 72.46% reduction in power , 70.11% reduction in PDP at 1.8V with respect to standard 6T SRAM and 11.34% reduction in power , 27.48% reduction in PDP at 1.8V with respect to existing 9T SRAM as shown in table-I. The significant improvement at other voltages can be analysed from the Table-II and Table-III. The proposed circuit has been mainly designed for bit-interleaving application with better performances compared to earlier design of 9T SRAM in term of power, speed and PDP.

Table 1: - Power consumption and Delay of existing and proposed SRAM cell at 1.8V

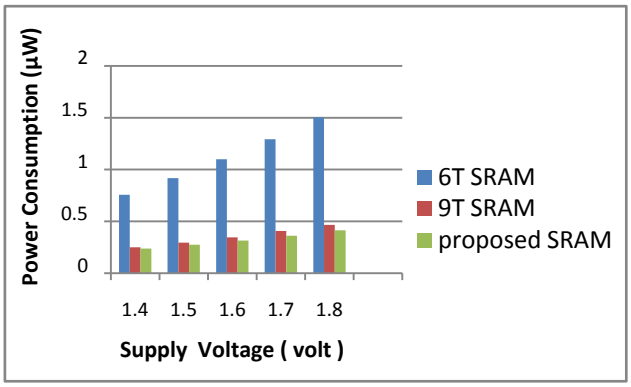
SRAM CELL	Power(µW)	Delay(pS)	PDP (fWS)
6T SRAM	1.504	48.12	72.372
9T SRAM	0.467	63.88	29.831
Proposed 13T SRAM	0.414	52.25	21.631

Table 2: - Power consumption and Delay of existing and proposed SRAM cell at 1.6V

SRAM CELL	Power(µW)	Delay(pS)	PDP (fWS)
6T SRAM	1.099	55.19	60.653
9T SRAM	0.346	67.89	23.489
Proposed 13T SRAM	0.315	57.43	18.090

Table 3: - Power consumption and Delay of existing and proposed SRAM cell at 1.4

SRAM CELL	Power(µW)	Delay(pS)	PDP (fWS)
6T SRAM	0.756	63.12	47.718
9T SRAM	0.250	73.90	18.475
Proposed 13T SRAM	0.238	64.37	15.320



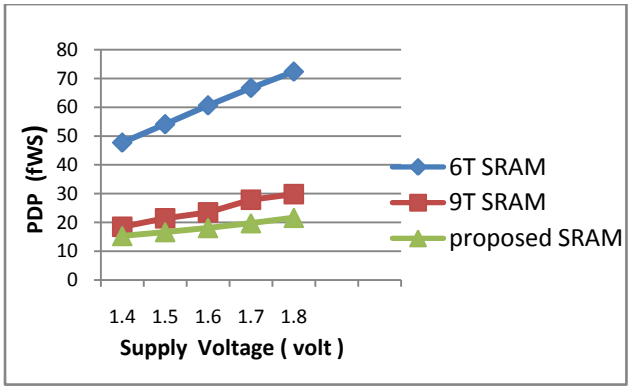


Fig 7: Variation of power and PDP with supply voltages

5. CONCLUSION

In this paper, a novel 13T SRAM cell with bit-interleaving capability has been proposed. The main motive of this paper is to reduce the average power consumption and leakage power. Analysis of results show that, the proposed 13T SRAM cell is giving better performance in terms of power consumption and PDP with respect to standard 6T SRAM cell and 9T SRAM with bit-interleaving capability. The delay of the circuit is increased slightly in comparison with that of standard 6T SRAM cell but PDP of the circuit reduces in significant amount while significant reduction in both delay and power consumption is observed with respect to 9T SRAM. Also the proposed circuit has bit-interleaving capability to reduce soft error probability.

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